Abstract

An electrical signal regenerator contains an equalizer and a clock data recovery circuit, whereby the latter is selected when an input signal of a higher bitrate multiplex level is detected and bypassed when an input signal of a lower bitrate multiplex signal is detected. This regenerator can advantageously be used in a bitrate-transparent asynchronous switch for signals of the new OTN according to ITU-T G.709. In particular, received optical signals undergo O/E conversion and are fed to an asynchronous space switching matrix operable to randomly switch signals from any to any port of the crossconnect. The switching matrix contains a number of switch modules electrically interconnected by means of internal electrical signal paths such as a backplane or electrical cables. An electrical signal regenerator is coupled to each input of a switching module.